PREFETCH CONTROL IN A DATA PROCESSING SYSTEM

Abstract of the Disclosure

In one embodiment, a data processing system (10) includes a first master, storage circuitry (35) coupled to the first master (12) for use by the first master (12), a first control storage circuit (38) which stores a first prefetch limit (60), a prefetch buffer (42), and prefetch circuitry (40) coupled to the first control storage circuit, to the prefetch buffer, and to the storage circuitry. In one embodiment, the prefetch circuitry (40) selectively prefetches a predetermined number of lines from the storage circuitry into the prefetch buffer (42) based on whether or not a prefetch counter, initially set to a value indicated by the first prefetch limit, has expired. In one embodiment, the first prefetch limit may therefore be used to control how many prefetches occur between misses in the prefetch buffer.